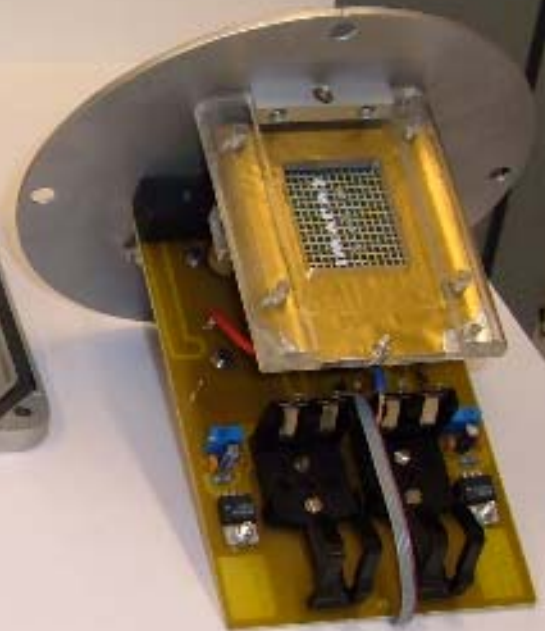
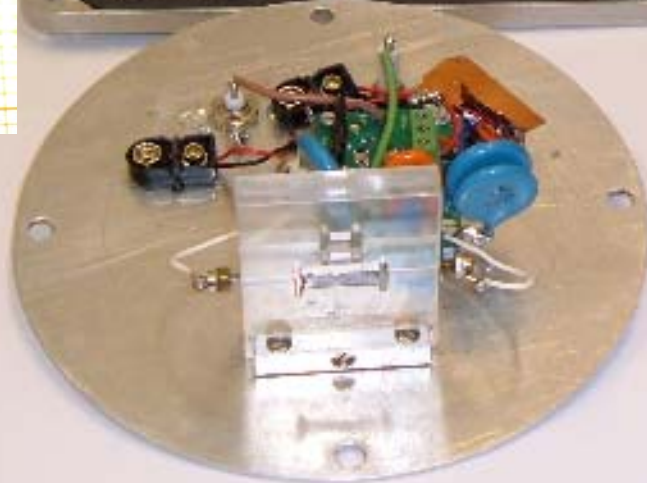
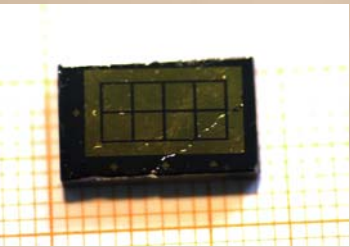


CZT detectors at IASF Milano



Roma, 18 Gennaio 2006

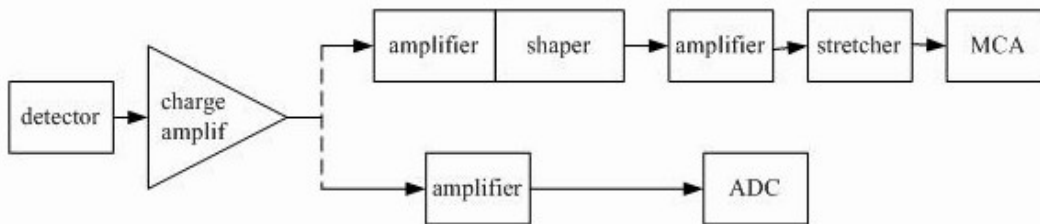
TEST SETUP



Cal. source support and detector assembly on the optical bench



The detector array mounted on the AFEE board

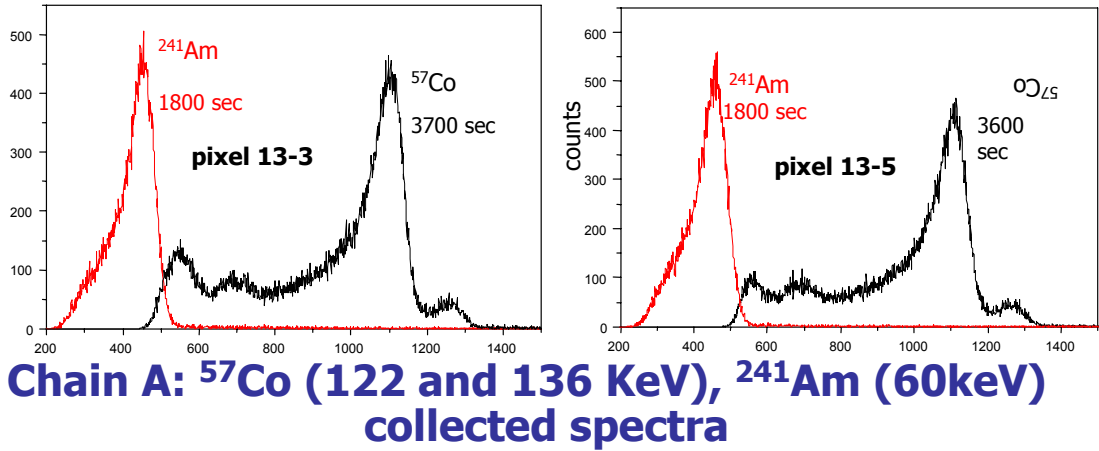


The signal analysis can be performed via two electronic chains

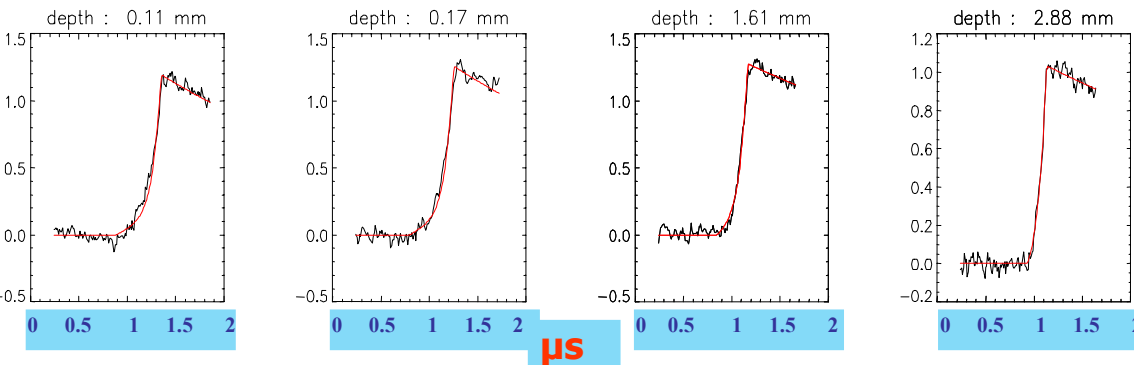
Performed tests:

- collect reference spectra
- analyse AFEE behaviour
- compare flash ADC chain wrt classical nuclear electronics
- check the correction algorithm.

TEST RESULTS



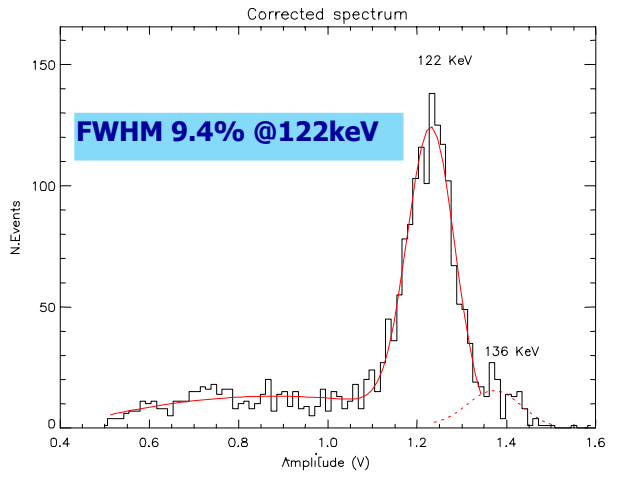
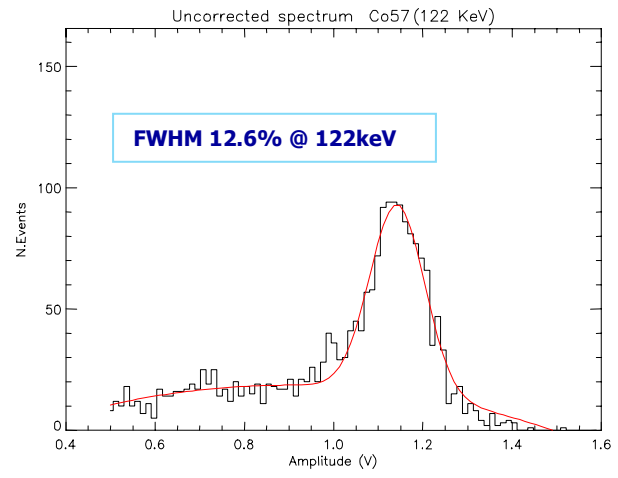
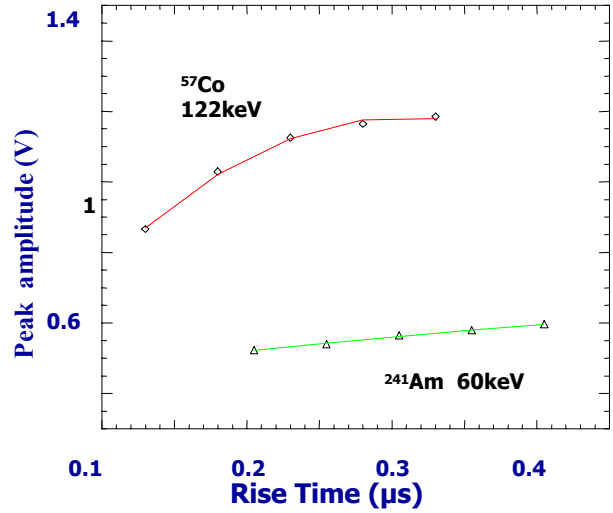
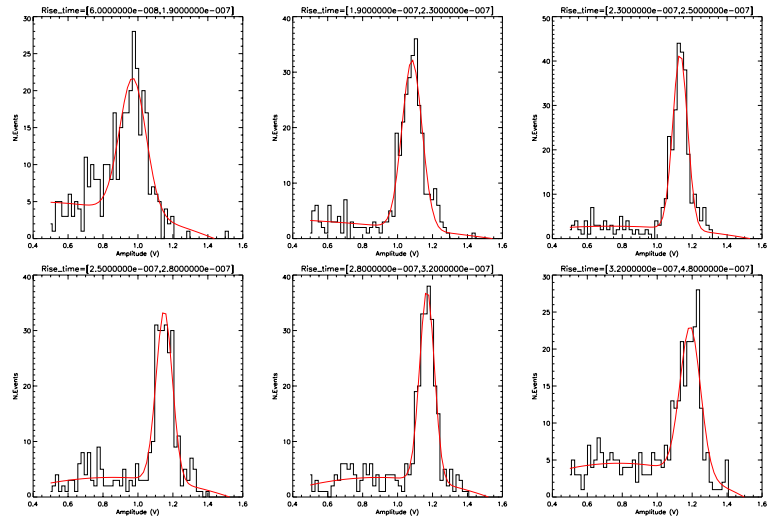
- The analytical model has been fitted to the recorded waveforms. Fit parameters:
- interacting photon energy
 - interaction depth
 - mobility lifetime ($\mu_e \cdot \tau_e$)



$$[\mu_h \cdot \tau_h = 1.2 \cdot 10^{-4}]$$

Best fit leads
 $\mu_e \cdot \tau_e = 3 \cdot 10^{-3} \text{ cm}^2/\text{V}$

TEST RESULTS

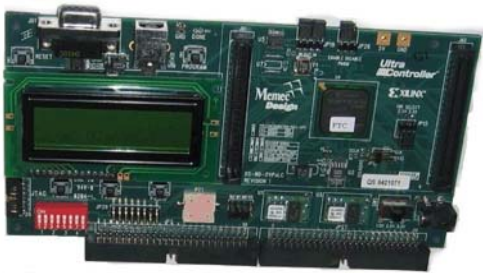


To correct the “tailing effect” we grouped wrt rise time the recorded waveforms.

The rise time binning has been chosen to have the same number of waveforms for each group, providing a proper SNR for each spectrum.

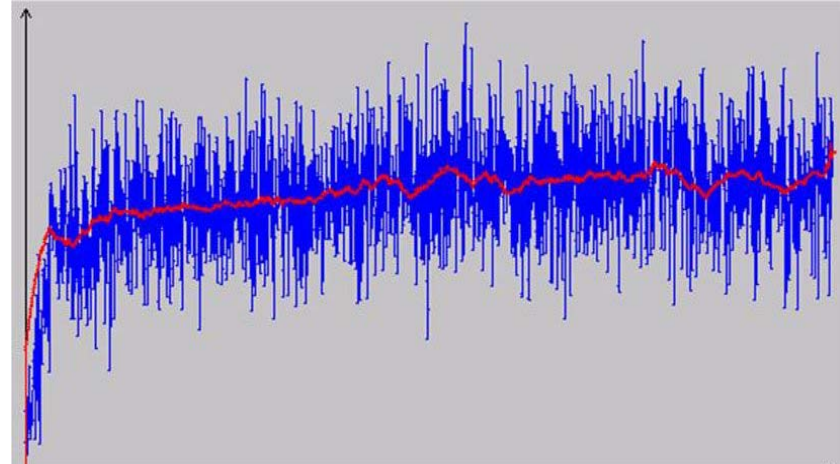
The dependence of the photo-peak centroid on the rise time has been used to correct the overall spectrum

The Mathematical model leads to algorithms for the best signal elaboration. These algorithms will be loaded in the DFE and performed in real time on the digital streams produced by the flash ADC.



The system used so far is based on the Xilinx XC2VP4 Virtex-II Pro FPGA embedding a PowerPC 405 processor. Signal processing algorithms are developed by C-language programs and compiled for the PowerPC.

At present, the FPGA board has been connected to a PC via the serial port, for algorithm evaluation purposes. In a second phase, the board will be connected directly to the digitalized output of the detector, for real-time analysis.



Moving average filter applied on a simulated input signal with superimposed noise.

CdZnTe crystal growing and detectors preparation at IMEM(CNR)

Present 1 inch crystals show big mono-crystal grains, up to 90% of the wafer (see figure below)

Hoven built at IMEM allows growing, with appropriate elements, crystal up to 3 inch.

IMEM is procuring supports, melting pot and other tools for growing 2 inch crystals.



CdZnTe crystal growing and detectors preparation at IMEM(CNR)

Up to now, CZT crystals with 10% Zn concentration (optimal for X-Gamma detectors) have been obtained.

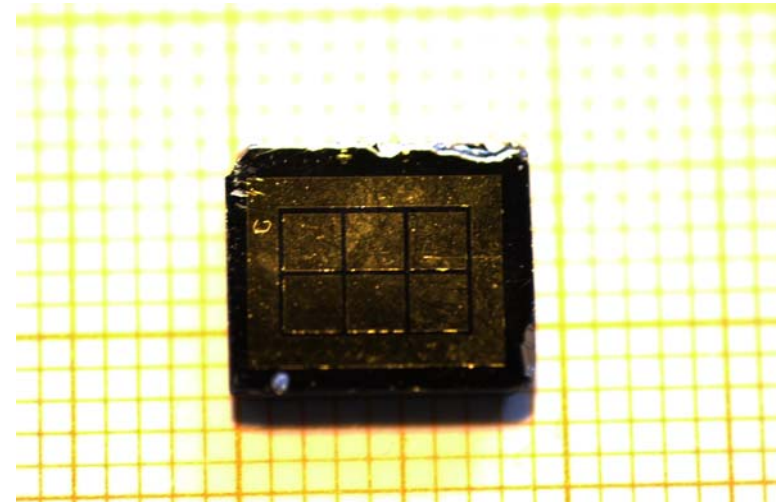
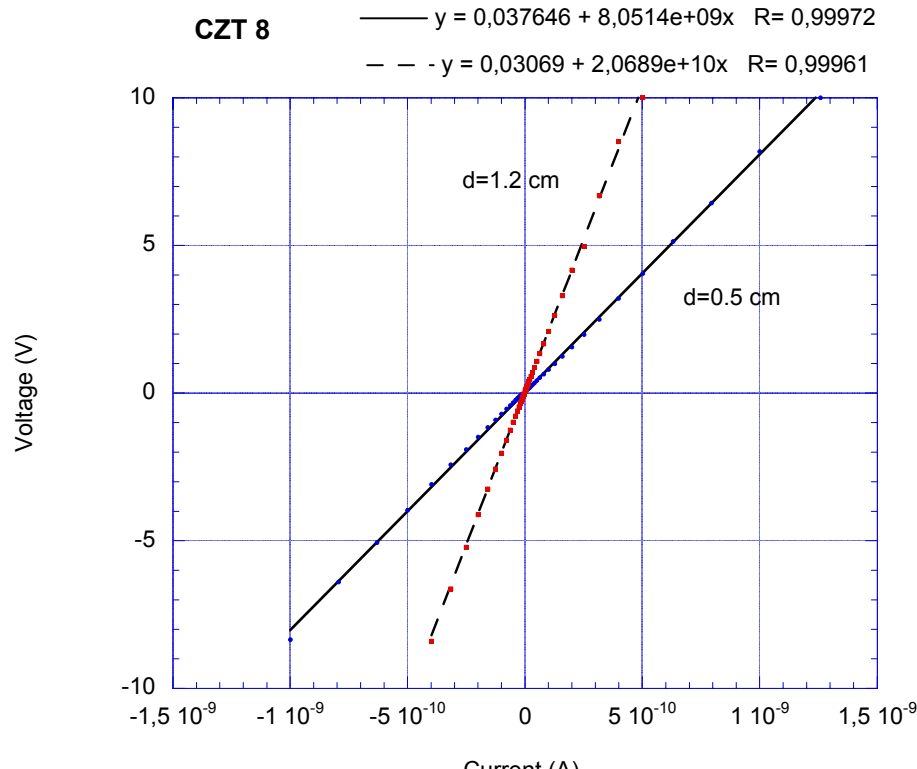
Last samples produced show resistivity greater than $10^{10} \Omega \text{ cm}$.

Crystals	Doping	Resistivity ($\Omega \text{ cm}$)
CdTe	Undoped	10^9
CZT4	Undoped	10^4
CZT5	In:doped*	$>10^9$
CZT6	In:doped*	$>10^{10}$
CZT7	In:doped*	$>10^{10}$
CZT8	In:doped*+Te Excess	$>10^{10}$

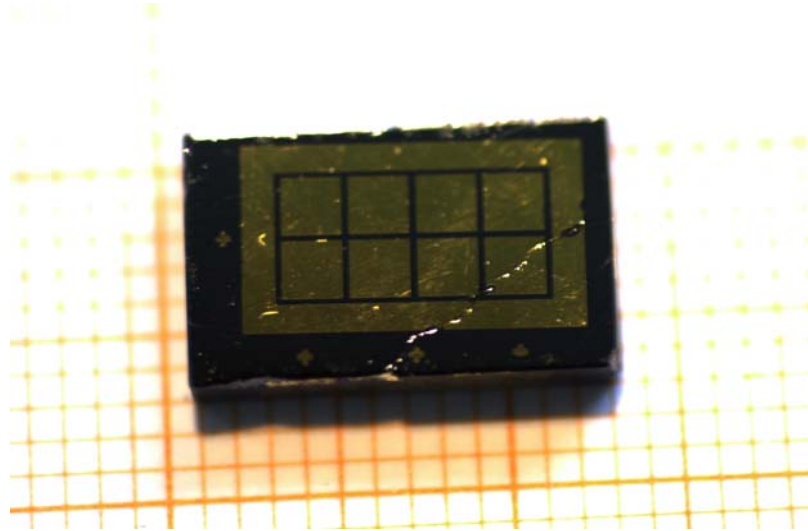
*($\cong 10^{16} \text{ atoms/cm}^3$)

CdZnTe crystal growing and detectors preparation

- Grown crystals led to first samples provided by pixels and guard ring.
- Contacts show good Voltage to Current characteristic.



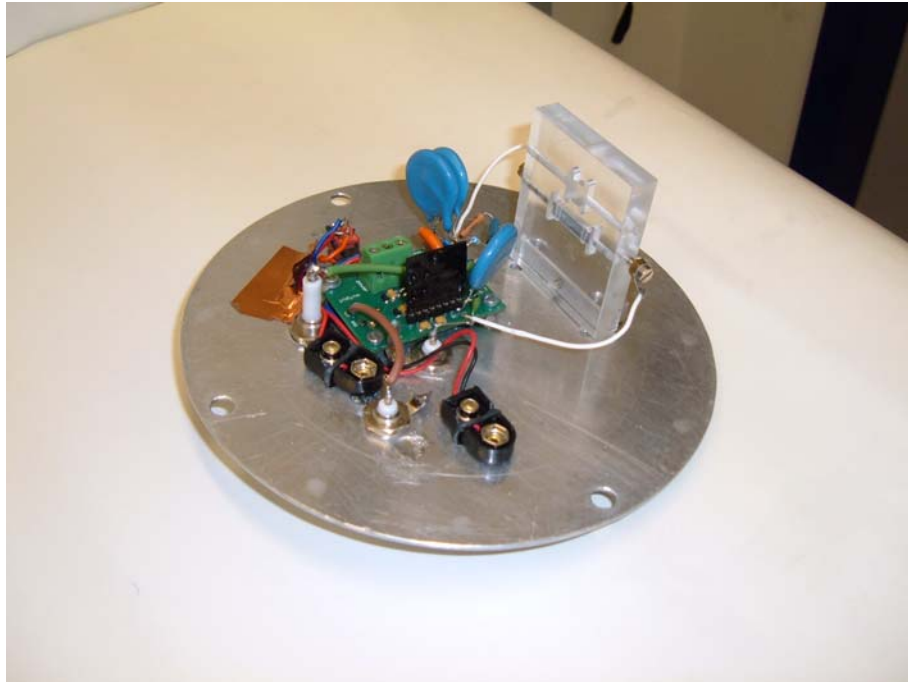
Rivelatori CZT per X- γ



Functional tests in progress. In next months all efforts will be devoted in improving techniques and procedures for:

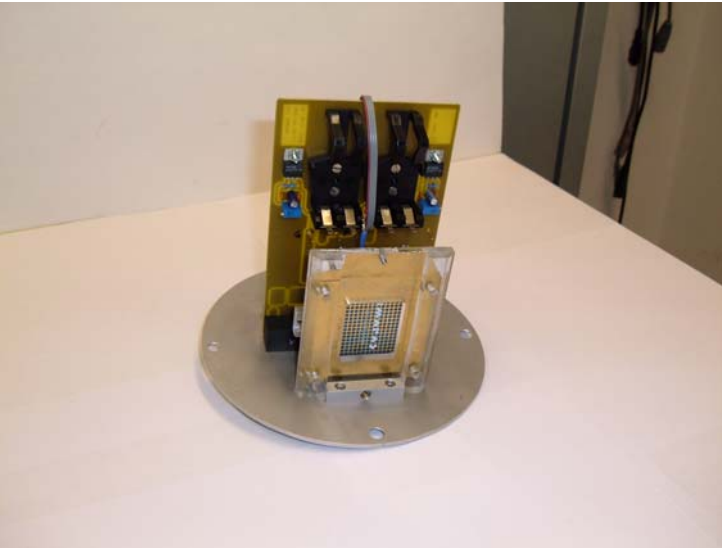
- » **Growing two inch crystals**
- » **Crystal cutting**
- » **Surface treatment and passivation**
- » **Contact deposition**
- » **bonding**
- » **Sample characterisation**
- » **Devices functional characterisation**

X- γ CZT detectors

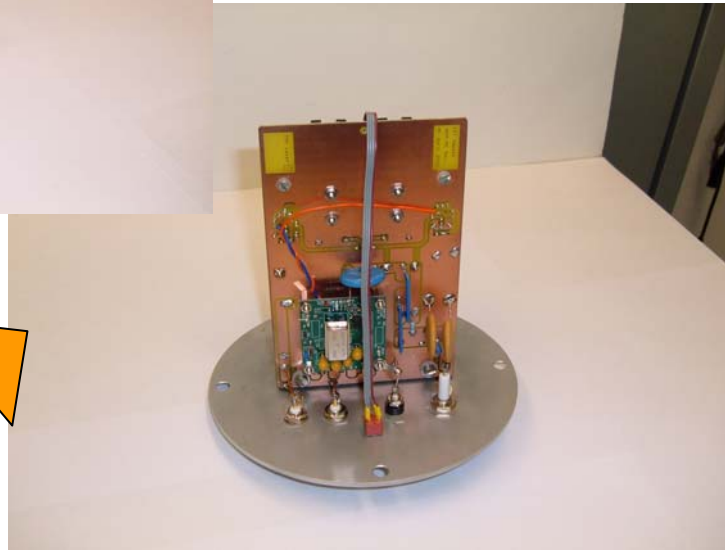
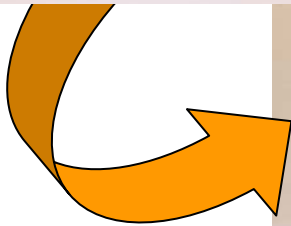


First prototype of AFEE:
IMARAD mono-pixel crystal +
charge preamplifier Cremat
CR110

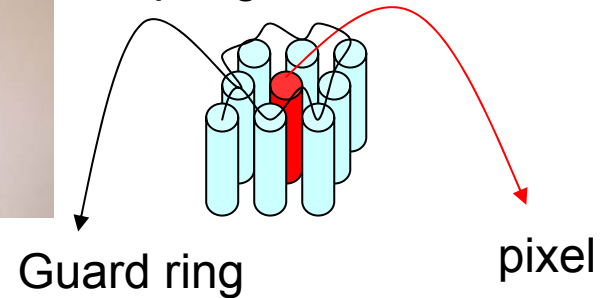
X- γ CZT detectors



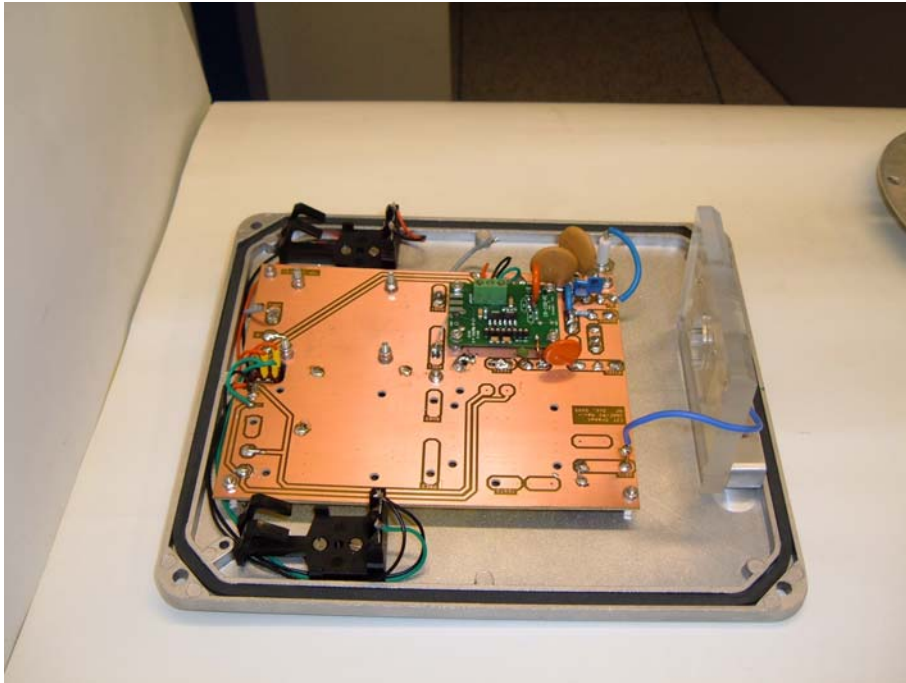
AFEE prototype based on Amptek A250 charge preamplifier. Single channel, pixel selectable among 256 pixels of a IMARAD 16x16 array



Selection of the pixel+guard ring with a mechanical system based on spring contacts:

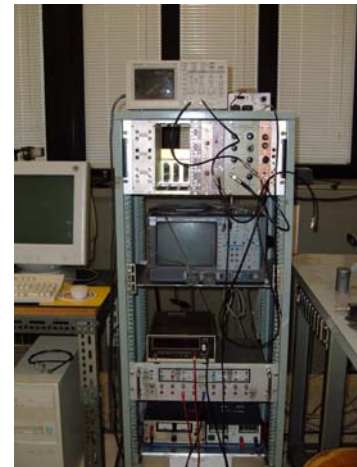


X- γ CZT detectors



Double channel AFEE (cross-talk analysis and energy reconstruction with anode/cathode differential signal)

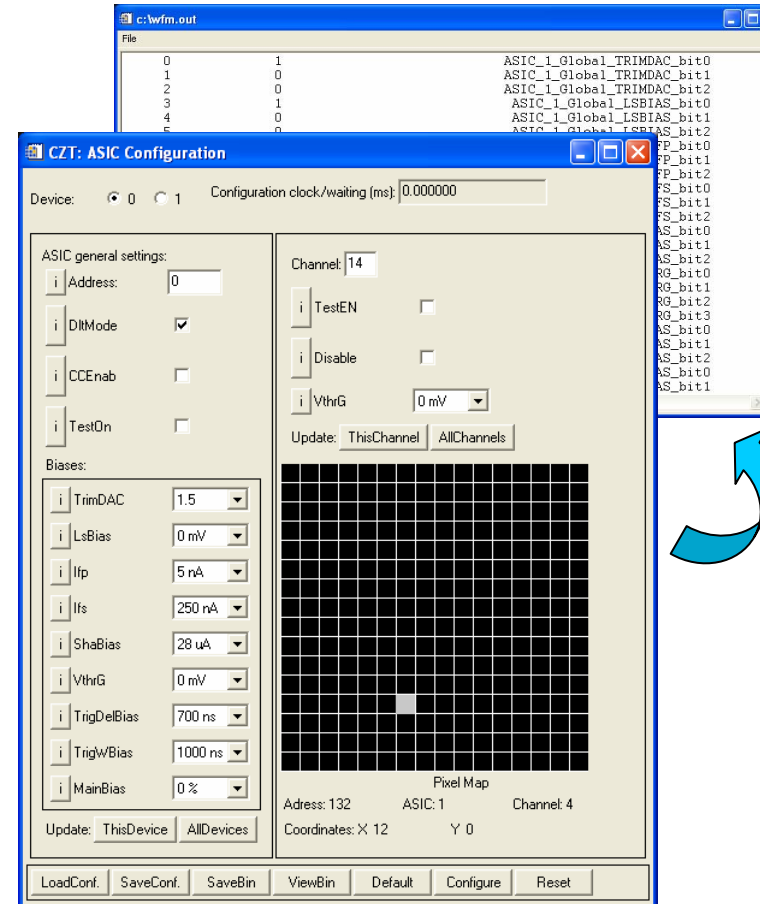
Work (and electronic setup) in progress ...



Prototype 16x16 pixels



Prototype IMARAD 16x16 pixels equipped with 2 ASICs IDEAS XAIM 3.3



Software GUI for ASICs configuration (developed in IDL 6.0)

X- γ CZT detectors

Electronic board design for the 16x16 pixels prototype

